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09/652,550	08/31/2000	Keiji Jono	KM1-001	4755

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EXAMINER
VU, QUANG D

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/652,550	JONO ET AL.	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 06/12/03* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11-32 and 62-68* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-32 and 62-68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *19* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,350,655 to Mizuo.

Mizuo (figures 1A-7) teaches a method of forming an isolation trench in a semiconductor comprising:

forming a first isolation trench portion (4) with a first gas mixture (column 8, lines 57-59), the first isolation trench portion (4) having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle (70°);

forming a second isolation trench portion (7) with a second gas mixture (column 9, lines 41-44) different from the first gas mixture, the second isolation trench portion (7) being formed within and extending below the first isolation trench portion (4), the second isolation trench portion (7) having a second depth and including a second sidewall intersecting the first sidewall at an angle (80°-90°) with respect to the surface that is greater than the first angle; and

filling the first (4) and second (7) isolation trench portions with dielectric material (10) (column 10, lines 3-8).

Mizuo teach forming the first isolation trench portion (4) comprises forming the first isolation trench portion having a first depth about 50 percent of a total trench depth (the depth of the first trench [4] is about 2000 Angstroms [column 9, lines 22-23]; the depth of the second trench [7] is about 2000 Angstroms [column 9, lines 59-60]; the total of [4] and [7] is about 4000 Angstroms [column 9, lines 60-62]).

Regarding claim 2, Mizuo teaches forming a second isolation trench portion includes forming the second angle about 80°-90° (column 9, lines 50-51).

Regarding claim 3, Mizuo teaches forming a first isolation trench portion (4) includes forming the first angle about 70° (column 8, lines 57-64) and forming a second isolation trench portion (7) includes forming the second angle about 80°-90° (column 9, lines 50-51).

Regarding claim 4, Mizuo teaches the semiconductor (1) comprises silicon (column 8, lines 40-41).

Regarding claim 12, Mizuo teaches forming the first isolation trench portion comprises forming the first isolation trench portion including a sidewall at least some of which forms a substantially straight linear segment.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5, 9, 13-17, 19-21 and 65-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,350,655 to Mizuo in view of US Patent No. 5,801,083 to Yu et al.

The disclosures of Mizuo are discussed as applied to claims 1-4 above.

Mizuo further teaches forming a silicon nitride layer (3) on the semiconductor surface (1). Mizuo differs from the claimed invention by not showing forming a masking layer having an opening disposed therein atop the silicon nitride layer, the opening including sidewalls. However, Yu et al. (figure 1) teach forming a photoresist layer (4) on the silicon nitride layer (3). Therefore, it would have obvious to one having ordinary skill in the art at the time the invention was made for forming a photoresist layer on the silicon nitride layer because it prevents damage for below layer. The combined device show forming a masking layer having an opening disposed therein atop the silicon nitride layer, the opening including sidewalls.

Mizuo differs from the claimed invention by not showing plasma etching through the silicon nitride layer using conditions that also deposit a polymer on the sidewalls; continuing etching for a predetermined time interval after the silicon nitride layer has been broached and continuing to deposit polymer on the sidewalls; and stopping the etching and depositing at the end of the predetermined time interval. However, Yu et al. (figures 1-3) teach forming a polymer layer (6b) on the sidewall. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Yu et al. into the device taught by Mizuo because it eliminates the top corner wraparound and protects the sidewalls against an etching attack from the etching gas. The combined device show plasma etching through the silicon nitride layer using conditions that also deposit a polymer on the

sidewalls; continuing etching for a predetermined time interval after the silicon nitride layer has been broached and continuing to deposit polymer on the sidewalls; and stopping the etching and depositing at the end of the predetermined time interval.

Regarding claim 9, the disclosures of Mizuo and Yu et al. are discussed as applied to claim 5 above. Yu et al. teach plasma etching through the silicon nitride layer using gases including CF_4 and CHF_3 (column 3, lines 10-12). Mizuo and Yu et al. differ from the claimed invention by not showing plasma etching through the silicon nitride layer using gases including CF_4 and CHF_3 in a ratio of $CF_4/CHF_3 = 0.11$ to 0.67. It would have been obvious to one having ordinary skill in the art at the time the invention was made for plasma etching through the silicon nitride layer using gases including CF_4 and CHF_3 in a ratio of $CF_4/CHF_3 = 0.11$ to 0.67, since it has been held that discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 15, Mizuo teaches forming the first isolation trench portion comprises forming the first isolation trench portion including a sidewall at least some of which forms a substantially straight linear segment.

5. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuo in view of Yu et al. as applied to claims 1-5 and 12 above, and further in view of US Patent No. 6,383,931 to Flanner et al.

The disclosures of Mizuo and Yu et al. are discussed as applied to claim 5 above, the combined device further teach providing a mixture of gasses chosen from CF_4 and CH F_3 (Yu et al.; column 3, lines 10-11). Mizuo and Yu et al. differ from the claimed invention by not

showing supplying radio frequency excitation to the mixture. However, Flanner et al. teach radio frequency (column 11, lines 38-45). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Flanner et al. into the device taught by Mizuo and Yu et al. because it is capable of withstanding the temperature and chemical environment of semiconductor manufacture.

Regarding claim 7, the disclosures of Mizuo, Yu et al. and Flanner et al. are discussed as applied to claim 6.

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuo in view of US Patent No. 6,258,688 to Tsai.

The disclosures of Mizuo are discussed as applied to claims 1-4 above.

Mizuo differs from the claimed invention by not forming the first isolation trench portion comprises plasma etching the first isolation trench portion using gases including CF_4 and CHF_3. However, Tsai teaches forming the isolation trench portion comprises plasma etching using compound gases of CF_4 and CHF_3 (column 5, lines 18-38). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Tsai into the method taught by Mizuo because it reduces the size of the trench.

Neither Mizuo nor Tsai teach forming the first isolation trench portion comprises plasma etching the first isolation trench portion using gases including CF_4 and CHF_3 in a ratio of $CF_4/CHF_3 = 0.11$ to 0.67. It would have been obvious to one having ordinary skill in the art at the time the invention was made for forming the first isolation trench portion comprises plasma etching the first isolation trench portion using gases including CF_4 and CHF_3 in a ratio of

CF_4/CHF_3 = 0.11 to 0.67, since it has been held that discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuo in view of US Patent No. 5,874,317 to Stolmeijer.

The disclosures of Mizuo are discussed as applied to claims 1-4 above.

Mizuo differs from the claimed invention by not planarizing the dielectric material filling the first and second isolation trench portions. However, Stolmeijer teaches planarizing the surface of the insulating layer (see figure 22). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Stolmeijer into the method taught by Mizuo, since it reduces the size of the device.

8. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuo in view of Yu et al. as applied to claims 5, 9 and 13-17 above, and further in view of US Patent No. 5,874,317 to Stolmeijer.

The disclosure of Mizuo and Yu et al. are discussed as applied to claims 5, 9 and 13-17 above.

Mizuo and Yu et al. differ from the claimed invention by not planarizing the dielectric material filling the first and second isolation trench portions. However, Stolmeijer teaches planarizing the surface of the insulating layer (see figure 22). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate

the teaching of Stolmeijer into the method collectively taught by Mizuo and Yu et al., since it reduces the size of the device.

9. Claims 22, 24, 27-30, 32 and 62-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,969,393 to Noguchi. in view of US Patent No. 6,274,457 to Sakai et al.

Noguchi (figures 2A-4B) teaches a method of forming an isolation trench isolated transistor comprising:

forming first and second trenches disposed to a respective side of a portion of silicon, forming the first and second isolation trenches;

filling the first and second isolation trench portions with dielectric material (103);

forming a gate (108) extending across the silicon portion from the first isolation trench to the second isolation trench; and

forming source and drain regions (109) extending between the first and second isolation trench portions, the source region being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side.

Noguchi differs from the claimed invention by not forming a mask on the surface, the mask including first and second openings corresponding to the first and second isolation trenches; forming a first isolation trench portion in each of the first and second openings, each first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle; and forming a second isolation trench portion within and extending below each of the first isolation trench portions, the second isolation trench portions

having a second depth and including a second sidewall intersecting a respective one of the first sidewalls at an angle with respect to the surface that is greater then the first angle. However, Sakai et al. teach forming a mask (column 9, line 42) on the surface, the mask including an opening corresponding to the isolation trench; forming a first isolation trench portion (a trench portion that has an angle of A1) in the opening, the first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle; and forming a second isolation trench portion (a trench portion that has an angle of A2) within and extending below the first isolation trench portion (a trench portion that has an angle of A1), the second isolation trench portion (a trench portion that has an angle of A2) having a second depth and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater then the first angle (see figures 7, 8a-d; column 9, line 25 – column 10, line 13).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the trench-forming method of Sakai et al. into the first and second isolation trench-forming methods of Noguchi because it provides good electrical characteristics to the device isolation region. The combined device show forming a mask on the surface, the mask including an opening corresponding to the isolation trench; forming a first isolation trench portion in the opening, the first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle; and forming a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater then the first

angle, the second isolation trench portion having a bottom portion of silicon at the second depth; doping the bottom portion of the second isolation trench portion.

Regarding claim 24, Noguchi teaches forming a silicon nitride layer (102) on the semiconductor surface (101). Noguchi differs from the claimed invention by not showing forming a masking layer having an opening disposed therein atop the silicon nitride layer, the opening including sidewalls. However, Sakai et al. (figure 9a) teach forming a masking layer (104) on atop the silicon nitride layer (103). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Sakai et al. into the device taught by Noguchi because it protects and prevents damage for below layer.

Regarding claim 27, the combined device teaches forming a first isolation trench portion comprises forming a first isolation trench portion having a first sidewall intersecting a surface of the semiconductor at an angle in a range of from about thirty degrees to about seventy degrees.

Regarding claim 28, the combined device teaches forming a first isolation trench portion comprises forming a first isolation trench portion including a side at least some of which forms a substantially straight linear segment.

Regarding claim 29, the combined device teaches forming a second isolation trench portion comprises forming a second isolation trench portion having a second sidewall forming an angle of more than eighty degrees with the surface.

Regarding claim 30, the combined device teaches forming the first isolation trench portion (Sakai et al.; a trench portion that has angle of A1) comprises forming the first isolation trench portion having a first depth about 3.75 to 37.5 percent of a total trench depth (the depth of the

first trench is about 30-300 nm [column 9, lines 43-44]; the depth of the second trench is about 50-500 nm [column 9, lines 60-62]; the total of first and second trench is about 80-800 nm). The combined device shows the first isolation trench portion having a first depth of between five and fifty percent of a total trench depth.

Regarding claim 32, the combined device teaches a gate comprising polysilicon ([108] of Noguchi).

Regarding claim 62, the combined device teaches the source region ([109] of Noguchi) is disposed adjacent only one side of the gate.

Regarding claim 63, the combined device teaches the drain region ([109] of Noguchi) is disposed adjacent only one side of the gate.

Regarding claim 64, the combined device teaches the source region and drain region are disposed directly opposite one another on opposite sides of the gate.

10. Claims 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi in view of Sakai et al. as applied to claims 22, 24, 27-32 and 62-64 above, and further in view of US Patent No. 5,801,083 to Yu et al.

The disclosures of Noguchi and Sakai et al. are discussed as applied to claims 22, 24, 27-32 and 62-64 above.

Noguchi and Sakai et al. differ from the claimed invention by not showing plasma etching through the silicon nitride layer using conditions that also deposit a polymer on the sidewalls; continuing etching for a predetermined time interval after the silicon nitride layer has been broached and continuing to deposit polymer on the sidewalls; and stopping the etching and

depositing at the end of the predetermined time interval. However, Yu et al. (figures 1-3) teach forming a polymer layer (6b) on the sidewall. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Yu et al. into the device taught by Mizuo because it eliminates the top corner wraparound and protects the sidewalls against an etching attack from the etching gas. The combined device show plasma etching through the silicon nitride layer using conditions that also deposit a polymer on the sidewalls; continuing etching for a predetermined time interval after the silicon nitride layer has been broached and continuing to deposit polymer on the sidewalls; and stopping the etching and depositing at the end of the predetermined time interval.

Regarding claim 26, Yu et al. teach etching using gases including CF_4 and CHF_3 (column 3, lines 5-12). Noguchi, Sakai et al. and Yu et al. differ from the claimed invention by not showing etching using gases including CF_4 and CHF_3 in a ration of $CF_4/CHF_3 = 0.11$ to 0.67. It would have been obvious to one having ordinary skill in the art at the time the invention was made for etching using gases including CF_4 and CHF_3 in a ration of $CF_4/CHF_3 = 0.11$ to 0.67, since it has been held that discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

11. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi and Sakai et al. as applied to claims 22, 24, 27-32 and 62-64 above, and further in view of US Patent No. 6,258,688 to Tsai.

Regarding claim 23, the disclosures of Noguchi and Sakai et al. are discussed as applied to claim 22 above.

The combined device teaches forming a first isolation trench portion (a trench portion that has an angle of A1) comprises etching the silicon surface. Noguchi and Sakai et al. differ from the claimed invention by not etching the silicon surface using gases including CF_4 and CHF_3 to form a first isolation trench portion. However, Tsai teaches forming the isolation trench portion comprises plasma etching using compound gases of CF_4 and CHF_3 (column 5, lines 18-38). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Tsai into the method taught by Noguchi and Sakai et al. because it reduces the size of the trench.

Noguchi, Sakai et al. and Tsai differ further from the claimed invention by not forming the first isolation trench portion comprises plasma etching the silicon surface using gases including CF_4 and CHF_3 in a ratio of CF_4/CHF_3 = 0.11 to 0.67. It would have been obvious to one having ordinary skill in the art at the time the invention was made to find the optimal ratio of the gases of CF_4 and CHF_3, since it has been held that discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

12. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi and Sakai et al. as applied to claims 22-24, 27-32, and 62-64 above, and further in view of US Patent No. 5,874,317 to Stolmeijer.

Regarding claim 31, the disclosures of Noguchi and Sakai et al. are discussed as applied to claims 22-24, 27-32 and 62-64 above.

Noguchi and Sakai et al. differ from the claimed invention by not planarizing the dielectric material filling the first and second isolation trench portions. However, Stolmeijer teaches planarizing the surface of the insulating layer (see figure 22).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Stolmeijer into the method taught by Sakai et al., since it reduces the size of the device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

qv
August 18, 2003

Shouxiang Hu

SHOUXIANG HU
PRIMARY EXAMINER